WHAT IS CLAIMED IS:

1. A circuit board comprising:

a substrate having a joining surface; and

a plurality of solder bumps disposed on said joining surface of said substrate in such a manner as to form a predetermined profiled line or surface pattern;

wherein said solder bumps have tops which are flat and leveled, and a coplanarity of said solder bumps is 0.5 μm or less per 1 mm.

2. A circuit board according to claim 1, further comprising circular pads interposed between said solder bumps and said substrate to serve as base layers of said solder bumps.

3. A circuit board according to claim 2, wherein said tops of said solder bumps have ~~nearly~~ circular flat surfaces which are smaller in diameter than said pads.

4. A circuit board according to claim 2, wherein said tops of said solder bumps have nearly circular flat surfaces which are substantially equal in diameter to said pads, and the height of said solder bumps is smaller than the diameter of said pads.

5. A method of producing a circuit board including a substrate having a joining surface, and a plurality of solder bumps disposed on the joining surface of the substrate in such a manner as to form a predetermined profiled line or surface pattern, wherein the solder bumps have tops which are flat and leveled, and a coplanarity of

the solder bumps is 0.5 μm or less per 1 mm, the method comprising the steps of:

placing masses of solder on said solder bumps, respectively;

disposing a control member in the form of a flat plate at a predetermined position above said masses of solder; and

forming said masses of solder into said solder bumps all at once by melting said masses of solder and allowing said control member to control the height of said solder bumps while flattening said tops of said solder bumps all at once.

6. The method according to claim 5, wherein pads are disposed on said joining surface of said substrate in such a manner as to form said profiled line or surface pattern, and said solder bumps are once formed on said pads, respectively and then pressed in such a manner as to allow said tops to become flat and leveled.

7. The method according to claim 5, wherein pads are disposed on said joining surface of said substrate in such a manner as to form said profiled line or surface pattern, and said solder bumps are once formed on said pads, respectively and then ground in such a manner as to allow said tops to be flattened and leveled.

8. A flattening and leveling jig for disposition above masses of solder mounted on a main surface of a circuit board for controlling the height of solder bumps into which the masses of solder are formed by being heated and melted, the jig comprising:

a control member having a planar surface for controlling the height of said solder bumps; and

a pair of leg members which are independent parts and disposed on the side of said planar surface of said control member for support of said control member and for positioning of said planar surface.

9. The flattening and leveling jig according to claim 8, wherein said leg members are so constructed and arranged as to allow said planar surface of said control member to be parallel to said main surface of said substrate when said flattening and leveling jig is disposed in place.

10. The flattening and leveling jig according to claim 9, wherein said leg members are made of wire.

11. The flattening and leveling jig according to claim 10, wherein said control member has on the side of said planar surface a pair of groove in which said leg members are fitted.